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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/613,541	07/07/2000	Atsushi Nakamura	1374.34189R00	9061

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EXAMINER	
WILLIAMS, ALEXANDER O	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/613,541	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *104-123* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *104-123* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/21/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 09/613541 Attorney's Docket #: 501.34189R))
Filing Date: 7/7/2000; The certified copy has been filed in parent Application No.

08/570646, filed on 5/25/1995 and 12/20/94.

Applicant: Nakamura et al.

Examiner: Alexander Williams

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/11/08 has been entered.

Applicant's Amendment, filed 2/11/08 has been acknowledged.

Claims 1-103 are cancelled.

The disclosure is objected to because of the following informalities: The related application information should be updated.

Appropriate correction is required.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29

USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 104-123 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 37-41 of copending Application No. 10/105236. Although the conflicting claims are not identical, they are not patentably distinct from each other because a semiconductor device comprising: a substrate having a first main surface and a second main surface opposite to the first main surface; a semiconductor pellet mounted on the first main surface of the substrate a plurality of electrode pads formed on the second main surface of the substrate; and a plurality of bonding wires for electrically connecting the bonding pads of the semiconductor pellet with the electrode pads; wherein the semiconductor pellet is mounted facedown on the substrate, the substrate has slits that extend from the first main surface to the second main surface and expose the bonding pads of the semiconductor pellet, the bonding wires extend through the slits in the substrate to connect the bonding pads and the electrode pads and bump electrodes are formed on said electrode pads.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not identify the foreign application for patent or inventor's certificate on which priority is claimed pursuant to 37 CFR 1.55, and any foreign application having a filing date before that of the application on which priority is claimed, by specifying the application number, country, day, month and year of its filing.

The reissue oath/declaration filed with this application is defective because it fails to contain the statement required under 37 CFR 1.175(a)(1) as to applicant's belief that the original patent is wholly or partly inoperative or invalid. See 37 CFR 1.175(a)(1) and see MPEP § 1414. Claims 26-90 have been cancelled and the at least one error upon which the reissue is based is defective.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 104-123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinrichsmeyer et al. (U.S. Patent # 4,996,587) in view of Kondo et al. (U.S. Patent # 5,438,478) and further in view of Akram et al. (U.S. Patent # 5,674,785) and in further view of Takier et al. (U.S. Patent # 5,422,435).

For example, in claims 104 and similar claims 109, 114, 116, 118, 120, and 122, Hinrichsmeyer et al. (figures 1 to 7) specifically **figure 5** show a semiconductor device **20** comprising: a rigid substrate **10** having a first main surface and a second main surface opposite to the first main surface; a semiconductor pellet **19** mounted on the first main surface **23** of the rigid substrate, the semiconductor pellet having a plurality of semiconductor circuit elements (inherit) and a plurality of bonding pads **21**; a plurality of electrode pads formed on the second main surface of the rigid substrate; and a plurality of bonding wires **22** for electrically connecting the bonding pads of the semiconductor pellet with the electrode pads; wherein the semiconductor pellet is mounted facedown on the rigid substrate, the rigid substrate has slits **13** that extend from the first main surface to the second main surface and expose the bonding pads of the semiconductor pellet, the bonding wires extend through the slits in the rigid substrate to connect the bonding pads and the electrode pads and bump electrodes **25** are formed on said electrode pads. Hinrichsmeyer et al. fail to explicitly show a rigid substrate formed by glass fibers impregnated with epoxy or polyimide resins.

Kondo et al. is cited for showing electronic component carriers. Specifically, Kondo et al. (figures 1 to 32) specifically figures 3 and 4 discloses a semiconductor device comprising: a rigid substrate **10** having a first main surface and a second main surface opposite to the first main surface; a semiconductor pellet **34** mounted within the rigid substrate, the semiconductor pellet having a plurality of semiconductor circuit elements (inherit) and a plurality of bonding pads **(inherent)**; a plurality of electrode pads **28** formed on the second main surface of the rigid substrate; and a plurality of bonding wires **38** for electrically connecting the bonding pads of the semiconductor pellet with the electrode pads; wherein the semiconductor pellet is facedown in the rigid

substrate, the rigid substrate has slits **12** that extend from the first main surface to the second main surface and expose the bonding pads of the semiconductor pellet, the bonding wires connecting the bonding pads and the electrode pads; and the rigid substrate formed by glass fibers impregnated with epoxy or polyimide resins for the purpose of enhancing the lifetime and reliability of a connection between a chip and a substrate.

(2) FIG. 3 schematically shows a first embodiment of the electronic component carrier according to the invention. In FIG. 3, a printed wiring substrate 10 (thickness: 0.2 mm) formed by laminating copper foils onto both surfaces of a base material, which is obtained by impregnating a glass cloth with bismaleimide triazine resin, is provided at its central portion with a cavity 12 for mounting a given electronic component (e.g. semiconductor element) and through-holes 14 are formed in the substrate at given positions. The inner surface of the substrate constituting the through-hole 14 is first subjected to a copper plating and then to a nickel plating and further to a gold plating. On the other hand, a lead frame 20 composed of a given metal foil (e.g., MF202-H made by Mitsubishi Electric Corporation, thickness: 0.15 mm) is disposed on an upper surface of the substrate 10 in place, and a top portion of each inner lead 22 is subjected to a silver plating for the connection to a gold wire as mentioned later. Furthermore, an outer lead 24 is extended outward from the respective inner lead 22 in the lead frame so as to connect to the other circuit or the like in a given assembling operation. The printed wiring substrate 10 and the lead frame 20 are joined to each other through a layer 26 of an adhesive composed of an epoxy resin. The electronic component carrier shown in FIG. 3 corresponds to multipin-type QFP and is shown as only one piece of the lead frame for multiple pattern. As **the printed** wiring substrate, use may be made of a laminate of glass cloths each impregnated with a heat-resistant insulating resin such ***as epoxy resin, polyimide resin,*** Teflon (trade name) or the like, ceramic laminate and so on in addition to the above laminate covered at both surfaces with copper foils. In the embodiment of FIG. 3, a ground ring 28 for earth is connected to the conductor pattern formed on the rear surface side of the substrate 10 through the through-hole to reduce lead inductance, whereby the degree of freedom in the pattern design for the substrate 10 is improved.

(3) FIG. 4 shows a sectional view taken along a line IV--IV of FIG. 3. As shown in FIG. 4, the inner lead 22 of the lead frame

20 or the neighborhood thereof is joined to the front surface of the printed wiring substrate 10 through the adhesive layer 26 formed in place around the cavity 12. In this case, the substrate 10 is subjected to C-face working in order to improve the shapability in mold. The adhesive layer 26 is composed of a thermosetting resin having a high heat resistance such as epoxy resin, polyimide resin, triazine resin or the like. When the thermosetting resin is used as an adhesive, it is desirable that an amount of ionic impurities such as Cl.sup.- and so on is low (not more than 10 ppm).

Hinrichsmeyer et al. fail to explicitly show a height of said bump electrodes is greater than a thickness of said resin sealing body from said second surface of said substrate in a thickness direction of said semiconductor pellet.

Akram et al. (figures 1 to 11) specifically **figures 6 and 12C** discloses show a semiconductor device comprising: a substrate **12E** having a first surface, a second surface opposite to said first surface, electrode pads **90** formed on said second surface and a slit **(via within 12E)** passing through said substrate from said first surface to said second surface; a semiconductor pellet **18** having a circuit system and bonding pads (not shown, but inherent) formed on a main surface thereof, said semiconductor pellet being mounted over said substrate such said that said main surface of said semiconductor pellet is faced to said first surface of said substrate and said bonding pads are arranged in said slit in a plan view; bonding wires **32** electrically connecting said electrode pads of said substrate with said bonding pads of said semiconductor pellet via said slit; a resin sealing body **36E** sealing said bonding wires, said resin sealing body including a first portion on said first surface of said substrate, a second portion on said second surface of said substrate and a third portion in said slit, said first to third portions of said resin sealing body being formed in unitary to one another; and bump electrodes **16** formed on said second surface of said substrate such that said bump electrodes are electrically connected to said electrode pads of said substrate and a height of said bump electrodes is greater than a thickness of said resin sealing body from said second surface of said substrate in a thickness direction of said semiconductor pellet for the purpose of providing access for electrical interconnection through the interconnect opening alignments with bond pads on the die.

The combined references show the features of the claimed invention as detailed above, but fail to explicitly show the first and second bump electrodes being arranged to overlap with said semiconductor pellet in said plain view respectively.

Takiar et al. is cited for showing a stacked multi-chip modules and method of manufacturing. Specifically, Takiar et al. (figure 11) discloses show the first and second bump electrodes **236** being arranged to overlap with said semiconductor pellet **212** in said plain view respectively for the purpose of providing access for electrical interconnection through the interconnect opening alignments with bond pads on the die.

In claim 105, the combination with Hinrichsmeyer et al. show said row of bonding pads **21** is disposed at a substantially central area between said first pair of opposed edges of said semiconductor pellets.

In claim 106, the combination with Hinrichsmeyer et al. show wherein said semiconductor pellet **19** has a rectangular shape, and wherein said first pair of opposed edges correspond to a pair of longer edges and said second pair of opposed edges correspond to a pair of shorter edges.

In claim 107, the combination with Hinrichsmeyer et al. show wherein said slit **13** tapered so that an opening on said second surface of substrate is greater than an opening on said first surface of said substrate.

Therefore, it would be obvious to one of ordinary skill at the time of the invention to use Takier et al.'s overlapped first and second electrodes and use Akram et al.'s bump height greater than the resin and use Kondo et al's glass impregnated with epoxy or polyimide resin in the substrate and features to modify Hinrichsmeyer et al.'s substrate and features for the purpose of enhancing the lifetime and reliability of a connection between a chip and a substrate.

Response

Applicant's arguments filed 2/11/08 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,777,780,737,784,673,696,698,680,773	5/14/03 1/19/05 9/14/05 8/5/07 4/24/08
Other Documentation: foreign patents and literature in 257/778,777,780,737,784,673,696,698,680,773	5/14/03 1/19/05 9/14/05 8/5/07 4/24/08
Electronic data base(s): U.S. Patents EAST	5/14/03 1/19/05 9/14/05 8/5/07 4/24/08

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander O Williams/
Primary Examiner, Art Unit 2826

/AOW/
4/30/2008